

The diagram illustrates a system architecture divided into two main sections: the **HOST SIDE** and the **PANEL SIDE**, separated by a dashed line.

HOST SIDE:

- A **SYSTEM BUS** (13) is connected to a **GRAPHICS CHIP** (11).
- The **GRAPHICS CHIP** (11) is connected to **GRAPHICS MEMORY** (12) via a bus (14).
- The **GRAPHICS CHIP** (11) also includes an internal component (20).
- The **GRAPHICS CHIP** (11) is connected to a **DIGITAL I/F LINE** (49) via a component (15).

PANEL SIDE:

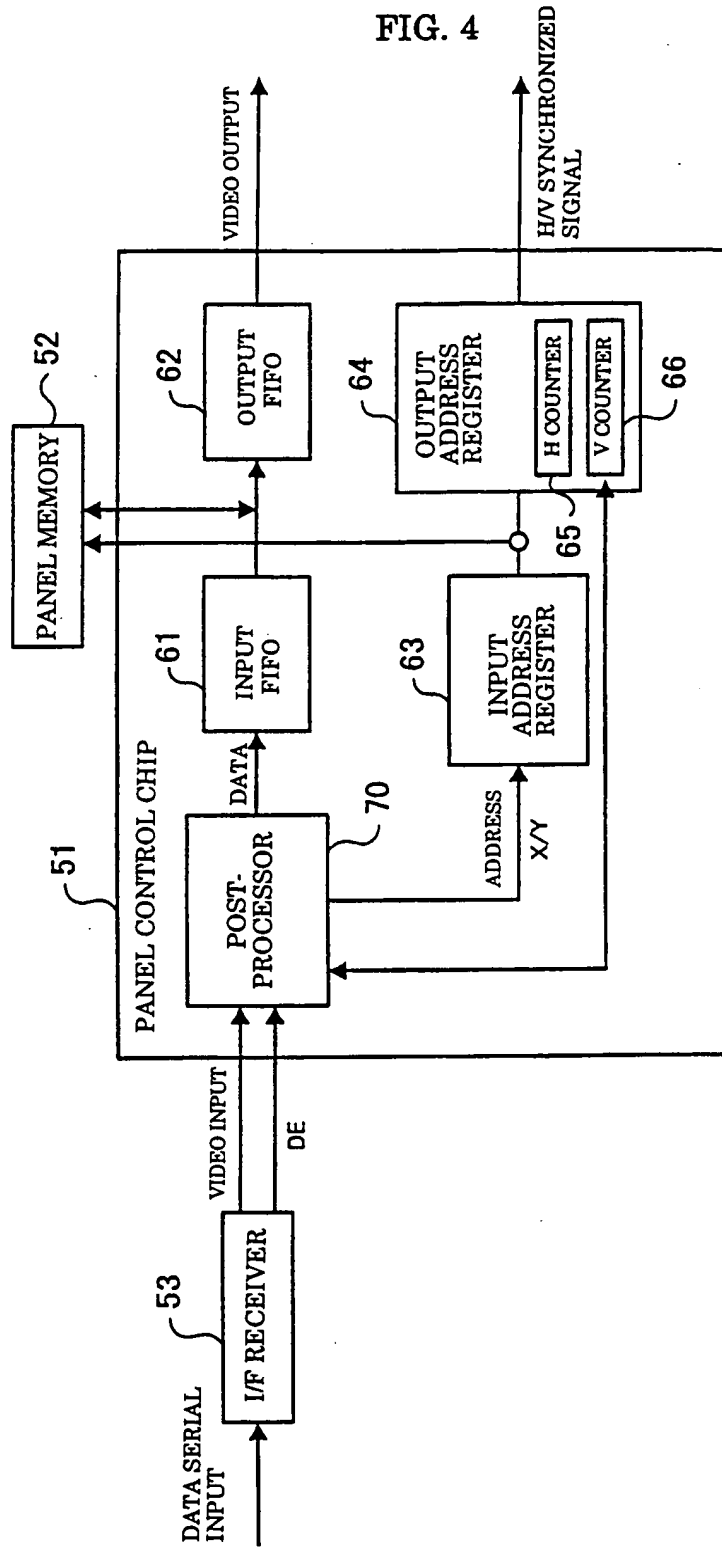
- The **DIGITAL I/F LINE** (49) connects to a component (53) on the panel side.
- There are four identical **PANEL CONTROL CHIP** (51) units.
- Each **PANEL CONTROL CHIP** (51) includes an internal component (70) and is connected to **PANEL MEMORY** (52).
- The **PANEL CONTROL CHIPS** (51) are connected to a common bus (68).
- The bus (68) is connected to a **PANEL** (54) via a component (69).
- The **PANEL** (54) is connected to the **PANEL CONTROL CHIPS** (51) via a bus (55).

The diagram illustrates a graphics chip (11) with the following components and connections:

- Internal Components:**
 - DAC (16):** Digital-to-Analog Converter, connected to the PRE-PROCESSOR.
 - PRE-PROCESSOR (20):** Receives data from the DAC and the ADDRESS GENERATOR. It outputs VIDEO OUTPUT and DE signals.
 - ADDRESS GENERATOR (17):** Outputs ADDRESS and DE signals to the PRE-PROCESSOR.
- External Connections:**
 - INTERFACE TRANSCEIVER (15):** Connected to the PRE-PROCESSOR and the DATA OUTPUT.
 - DDC:** Data Display Channel, connected to the PRE-PROCESSOR.

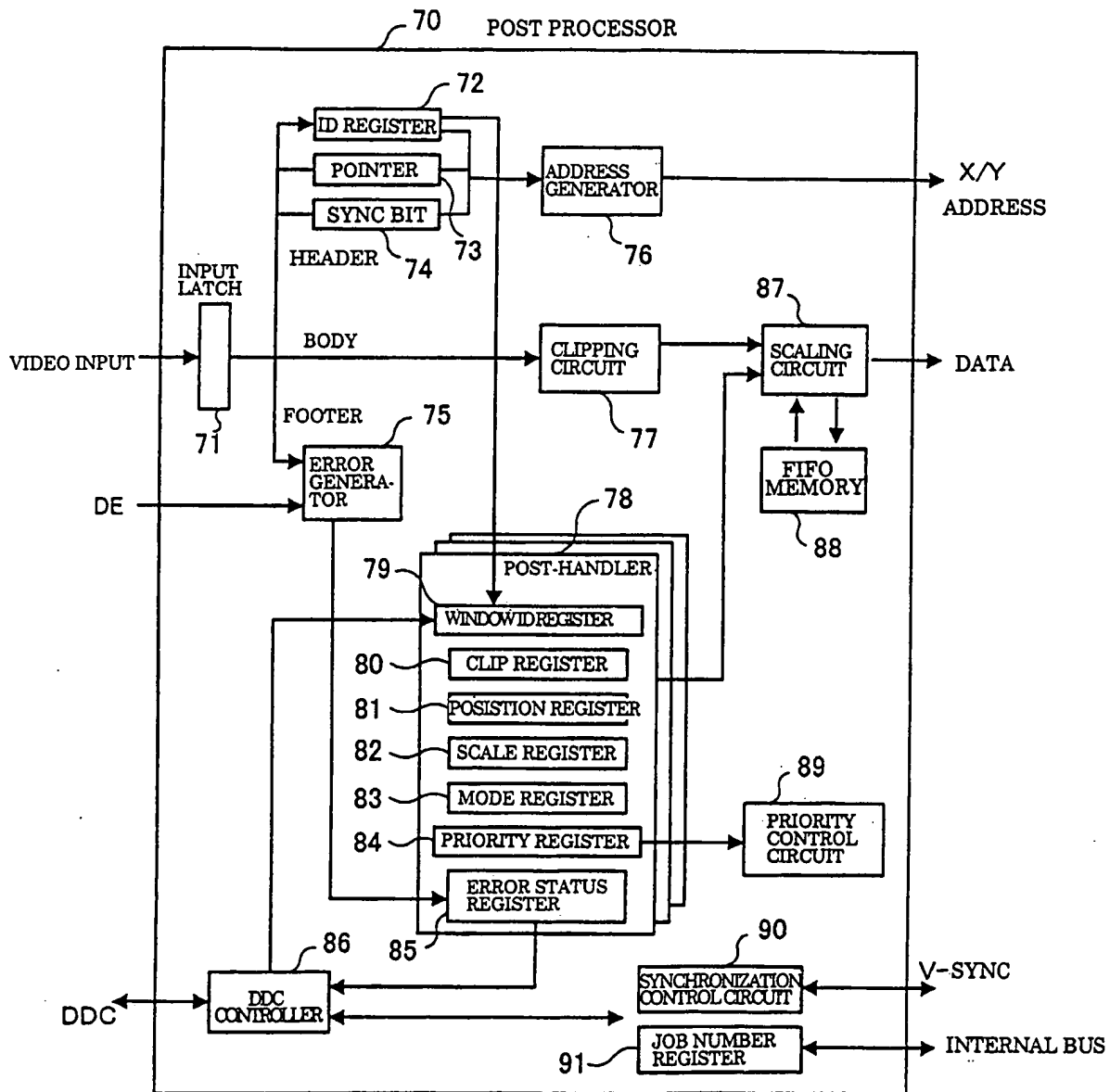
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FIG. 4



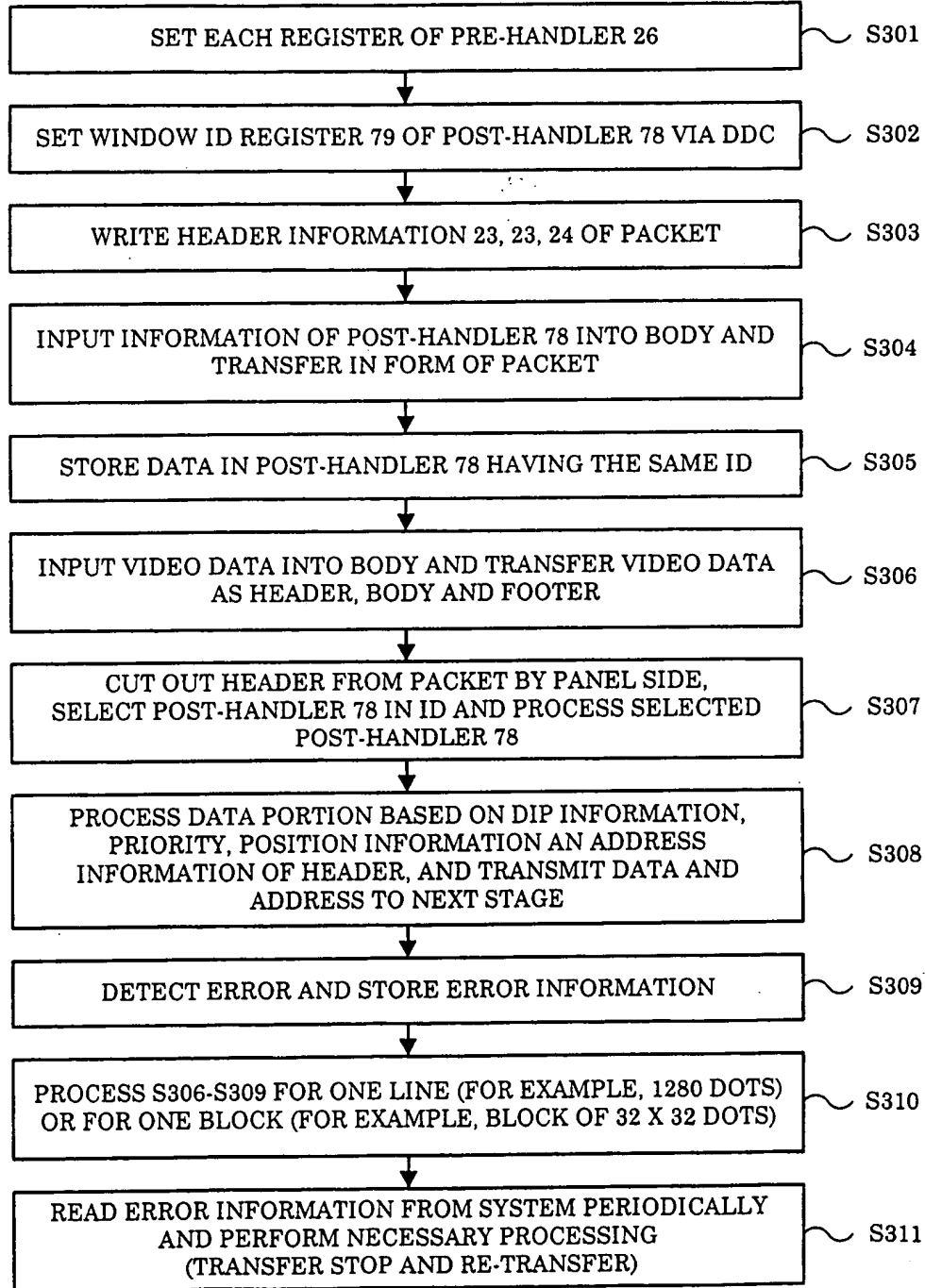
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FIG. 5



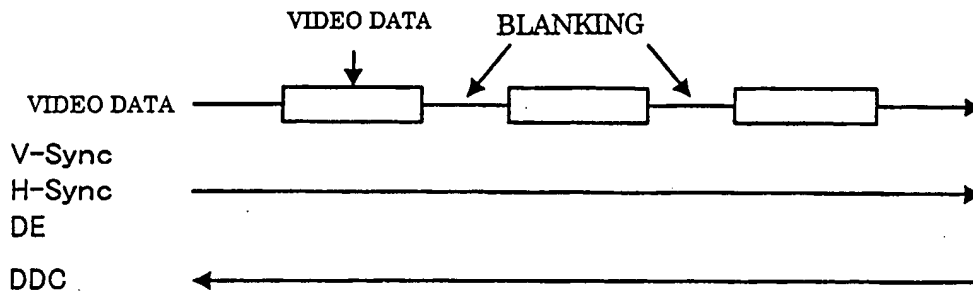
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FIG. 6

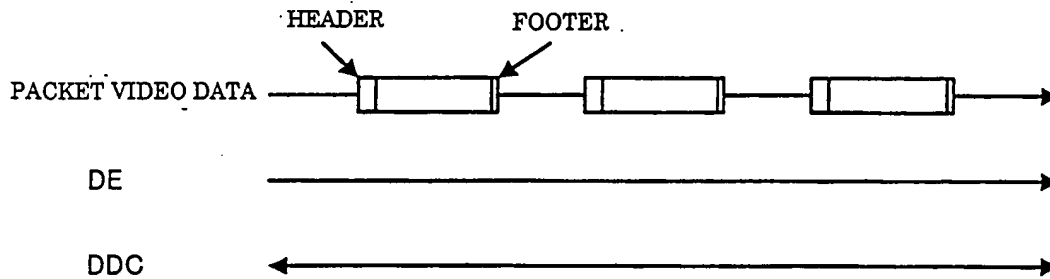


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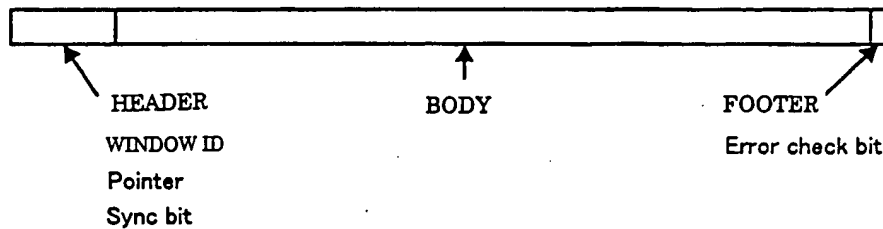
FIG. 7



(a) CONVENTIONAL TRANSFER OF VIDEO DATA



(b) TRANSFER OF VIDEO DATA IN THIS EMBODIMENT



(c) FORMAT OF PACKET VIDEO DATA

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FIG. 8

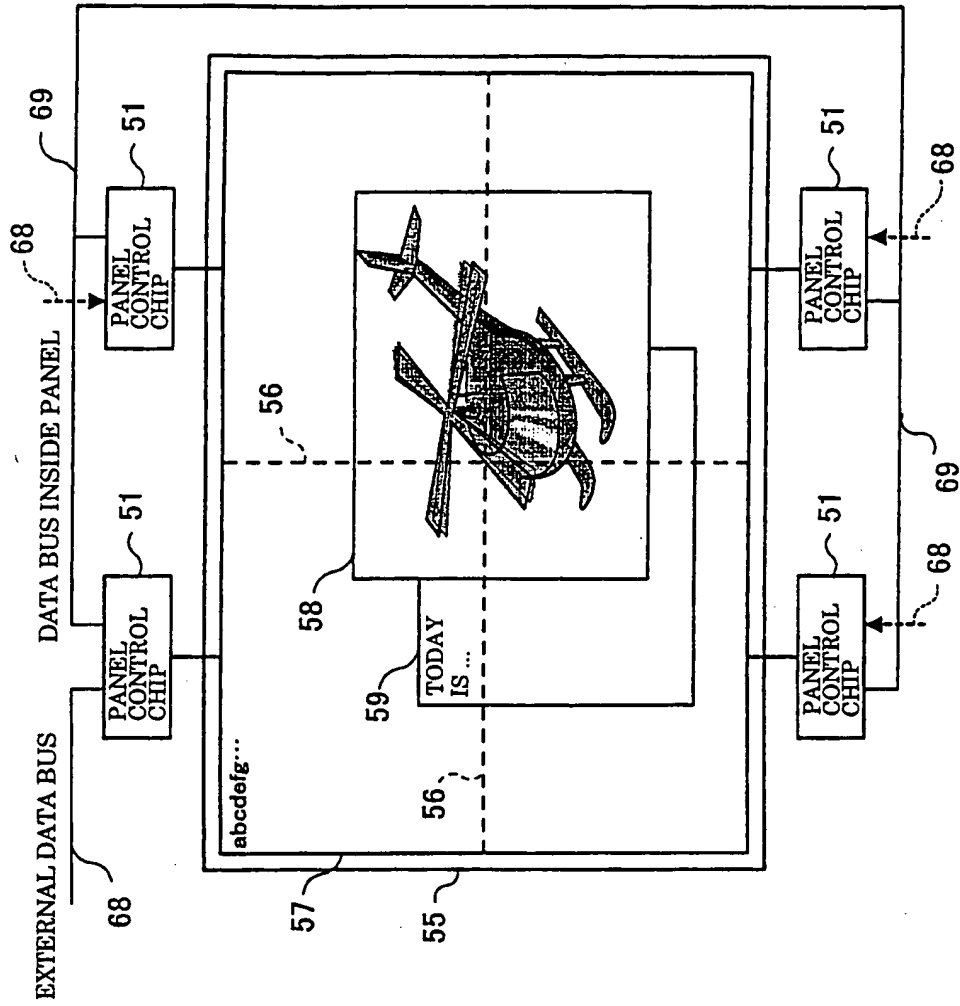
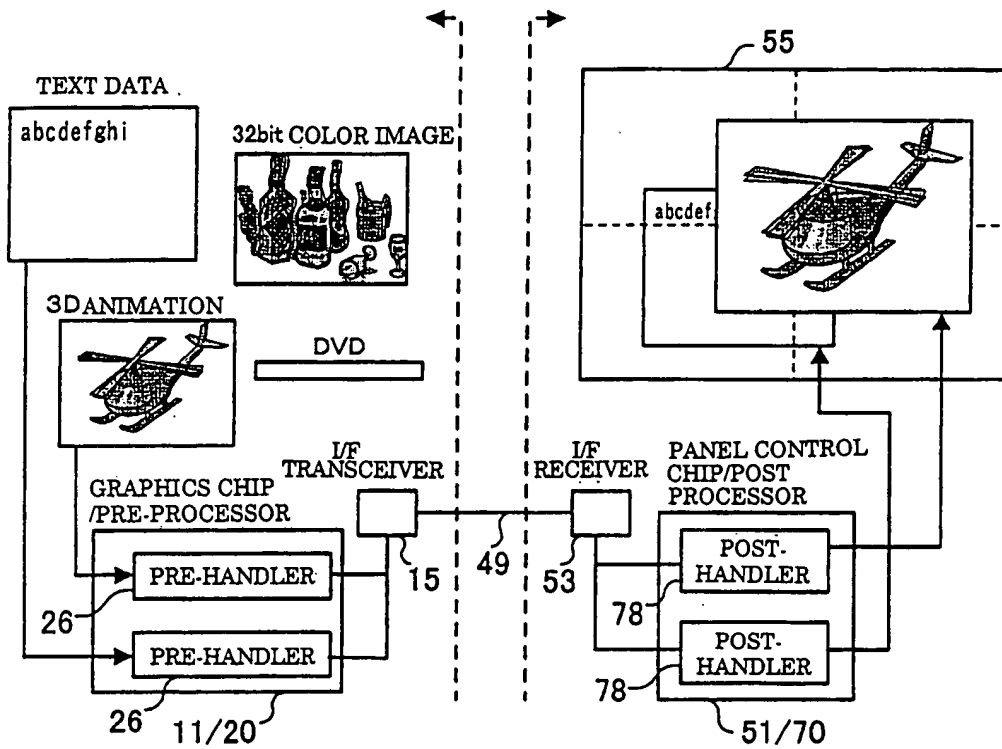
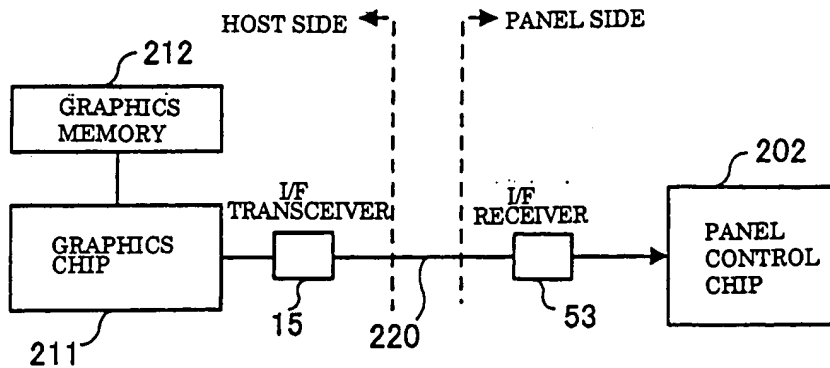


FIG. 9



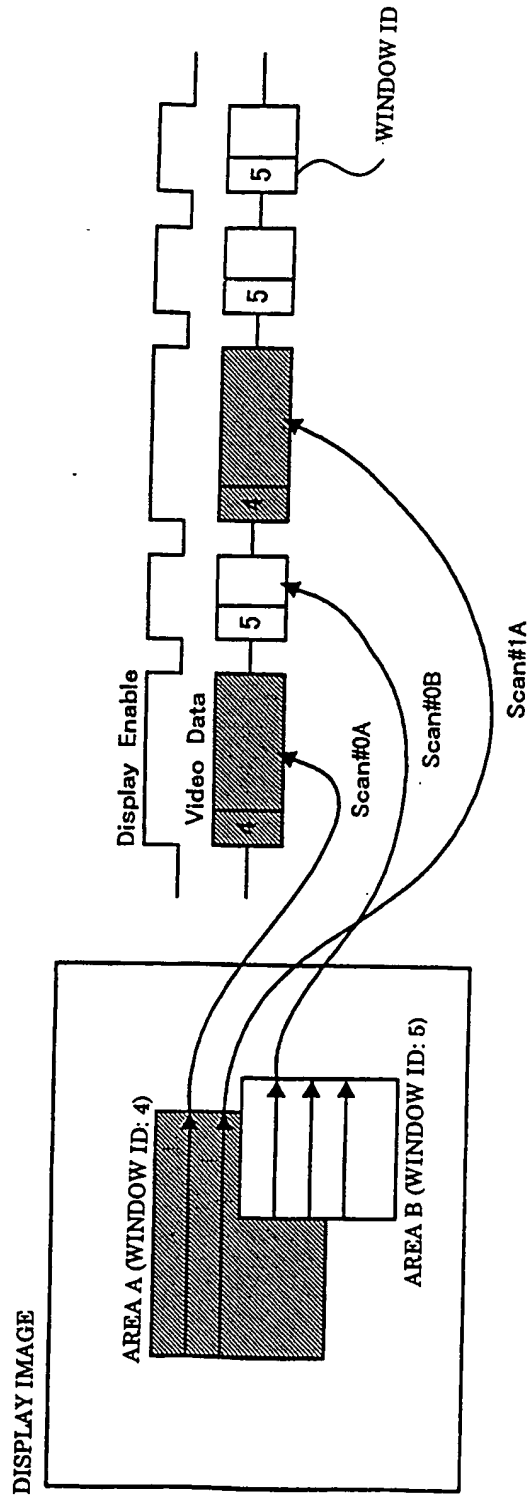
(a) DATA SOURCE AND PROCESSING SYSTEM



(b) LIMITATION OF DATA BAND WIDTH

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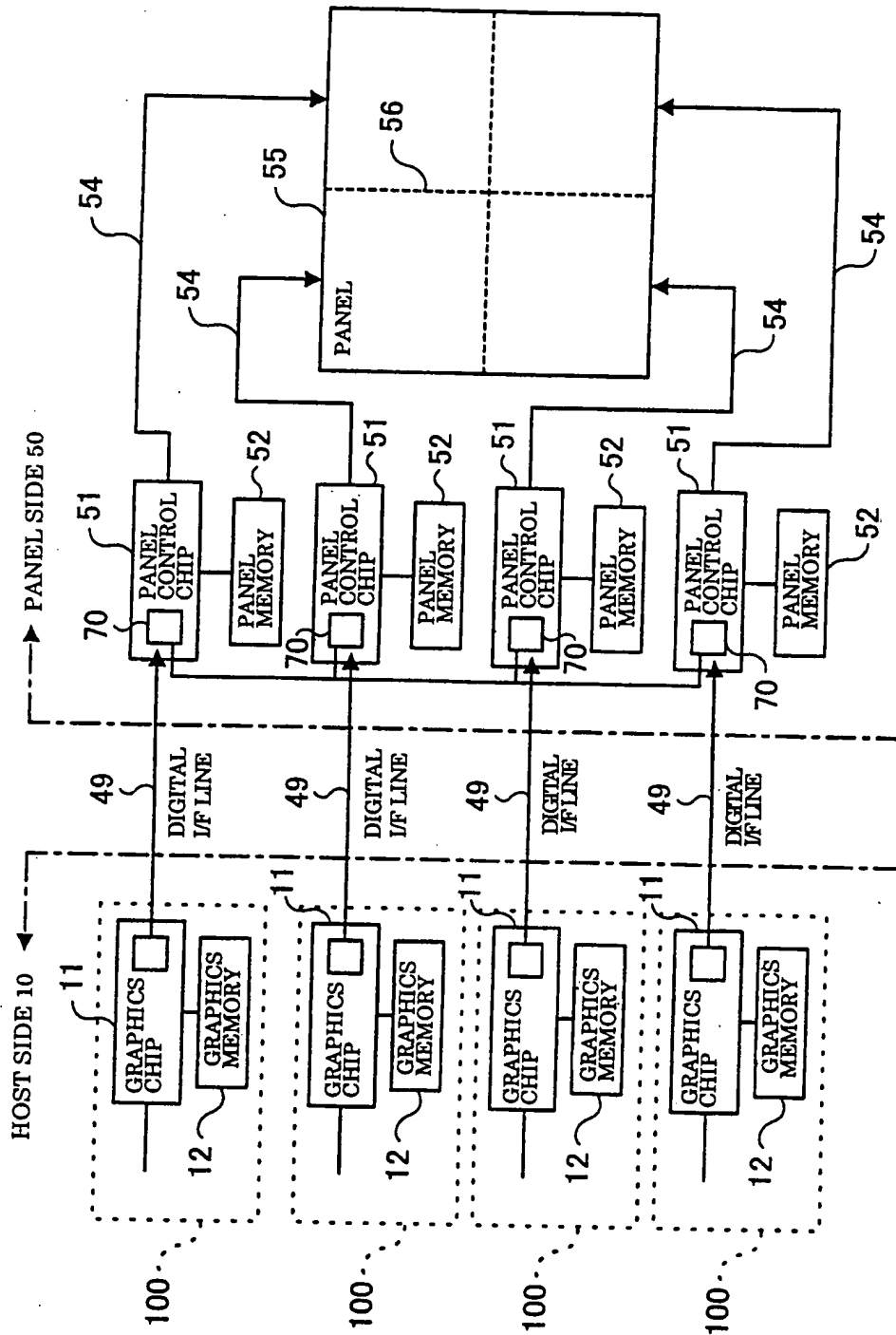
FIG. 10



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FIG. 11



The diagram illustrates a system architecture divided into two main sections: **HOST SIDE 10** and **PANEL SIDE 50**.

HOST SIDE 10: This section contains the **GRAPHICS CHIP/PRE-PROCESSOR** (11/20). It includes a **SYNCHRONIZATION CONTROL CIRCUIT** (43) with an **OFFSET REGISTER** (41), an **ADDER** (42), a **MULTIPLEXER** (44), and a **VERTICAL SYNCHRONIZATION COUNTER** (45). The circuit is connected to **H-Sync** and **INT_VSYNC** signals. It also features a **DDC HANDLER** (37) and a **READ/WRITE CONTROL** (45) block. The **DDC HANDLER** (37) is connected to **JOB NO. OUTPUT REGISTER** (33) and **JOB NO. INPUT REGISTER** (34). The **READ/WRITE CONTROL** (45) is connected to the **to CPU** interface.

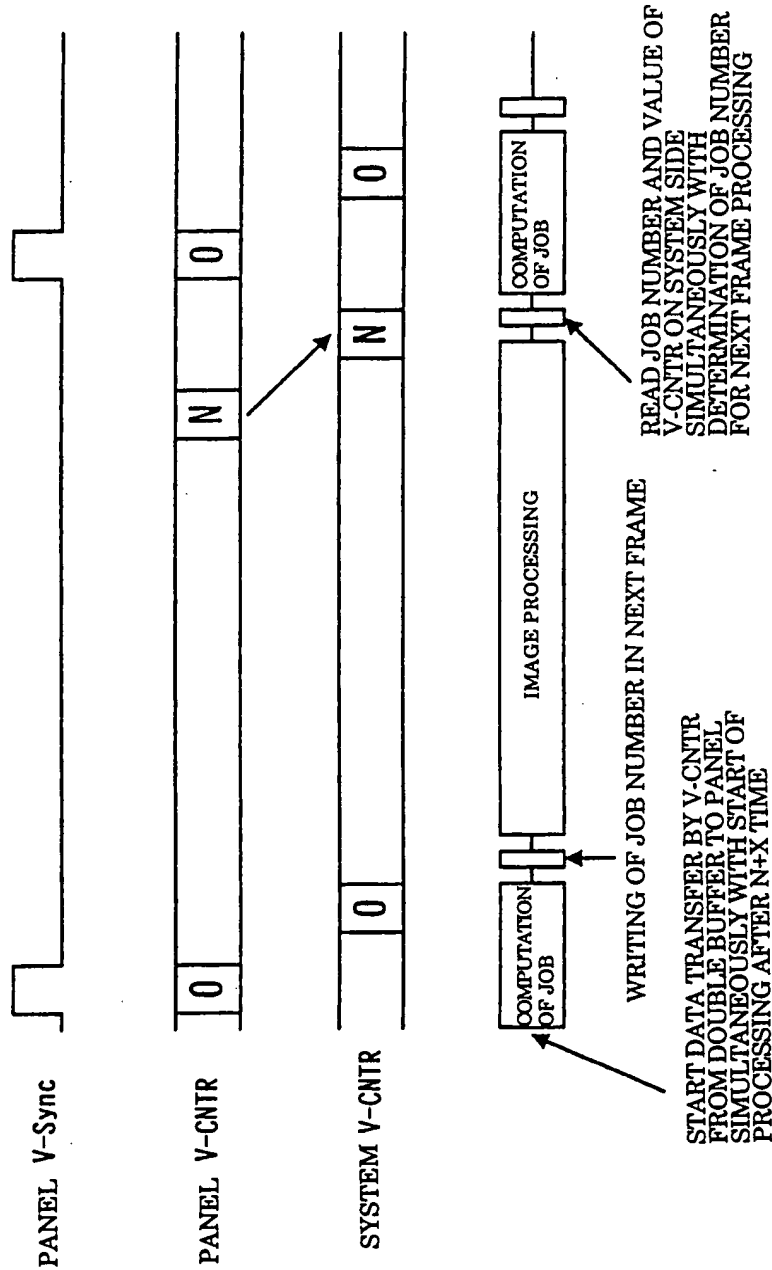
PANEL SIDE 50: This section contains the **PANEL CONTROL CHIP/POST PROCESSOR** (51/70). It includes a **SYNCHRONIZATION CONTROL CIRCUIT** (113) with an **OFFSET REGISTER** (113), an **ADDER** (114), and a **VERTICAL SYNCHRONIZATION COUNTER** (112). The circuit is connected to **INT_HSYNC** and **INT_VSYNC** signals. It also features a **DDC HANDLER** (115) and a **COMPARATOR** (119). The **DDC HANDLER** (115) is connected to **JOB NO. OUTPUT REGISTER** (117) and **JOB NO. INPUT REGISTER** (118). The **COMPARATOR** (119) is connected to the **INTERNAL BUS CONTROLLER** (120) and the **INT_BUS** (121).

Interconnections: A **DDC** line connects the **DDC HANDLER** (37) on the host side to the **DDC HANDLER** (115) on the panel side. The **INTERNAL BUS CONTROLLER** (120) is connected to the **INT_BUS** (121).

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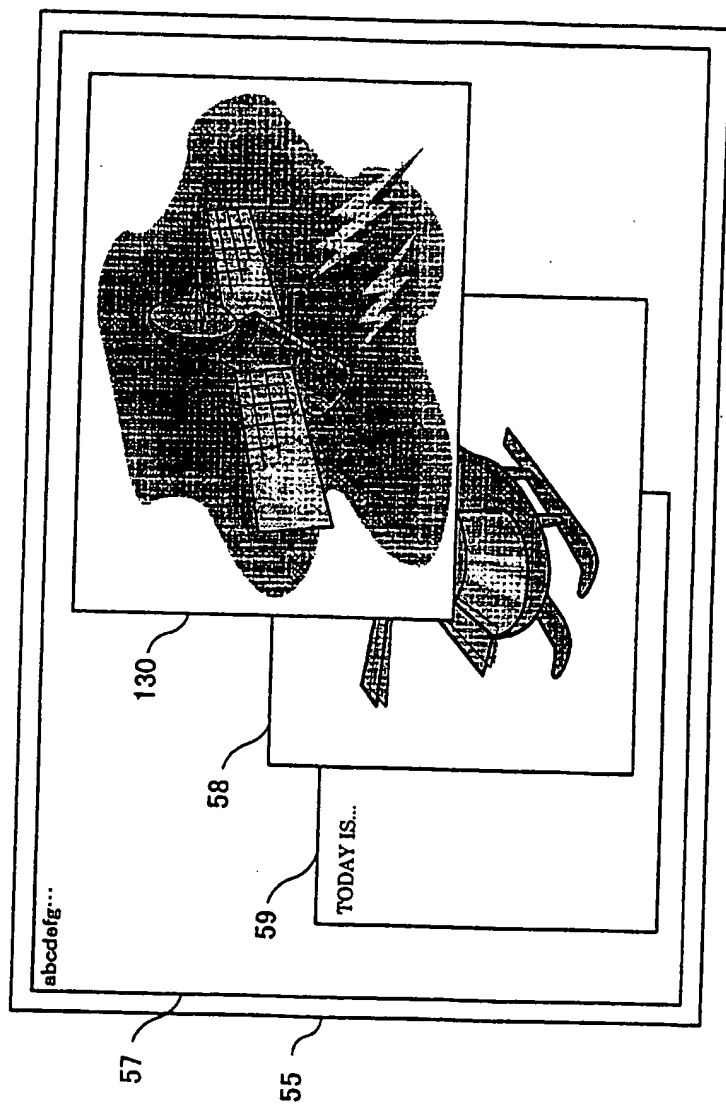
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FIG. 14



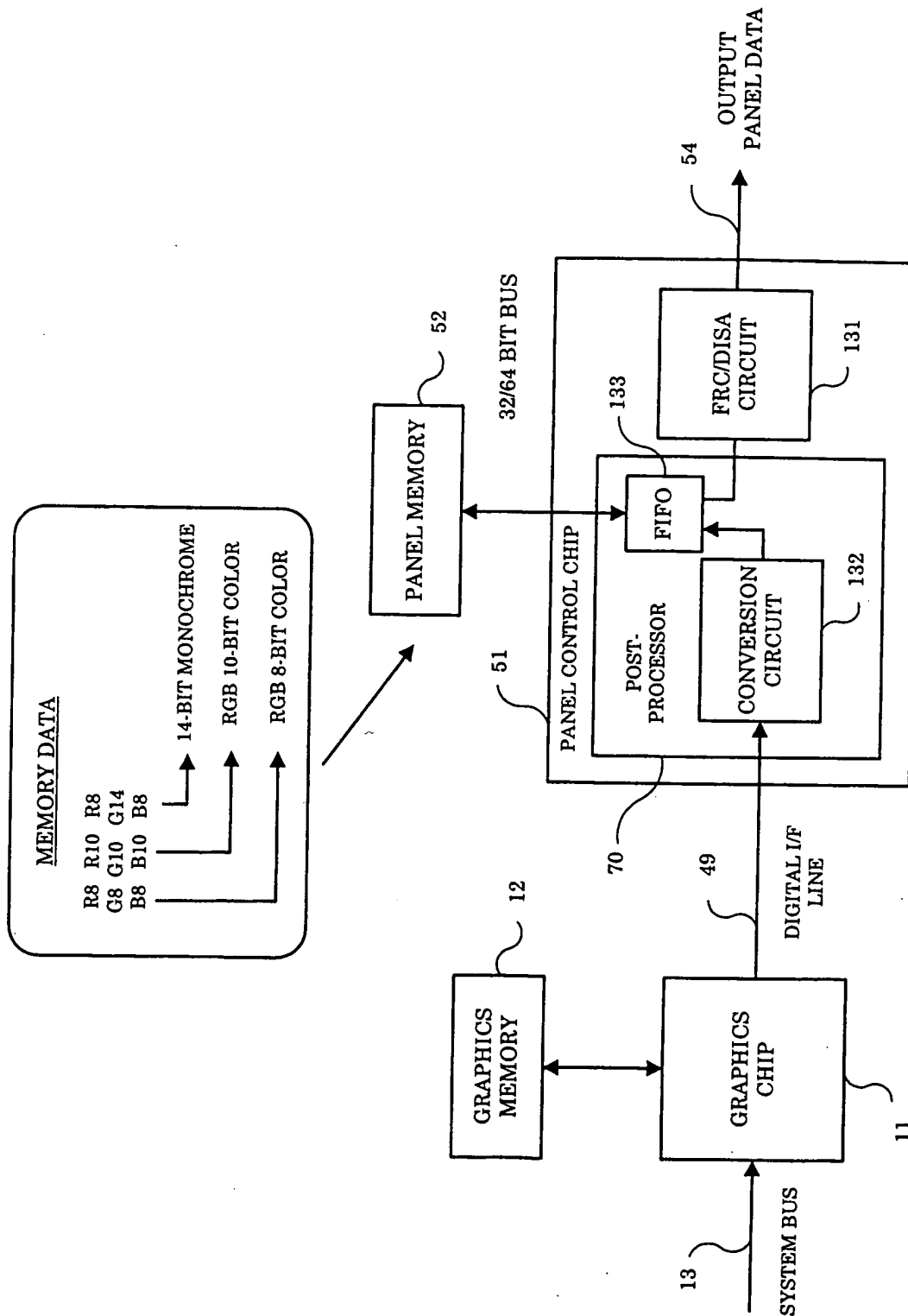
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FIG. 15



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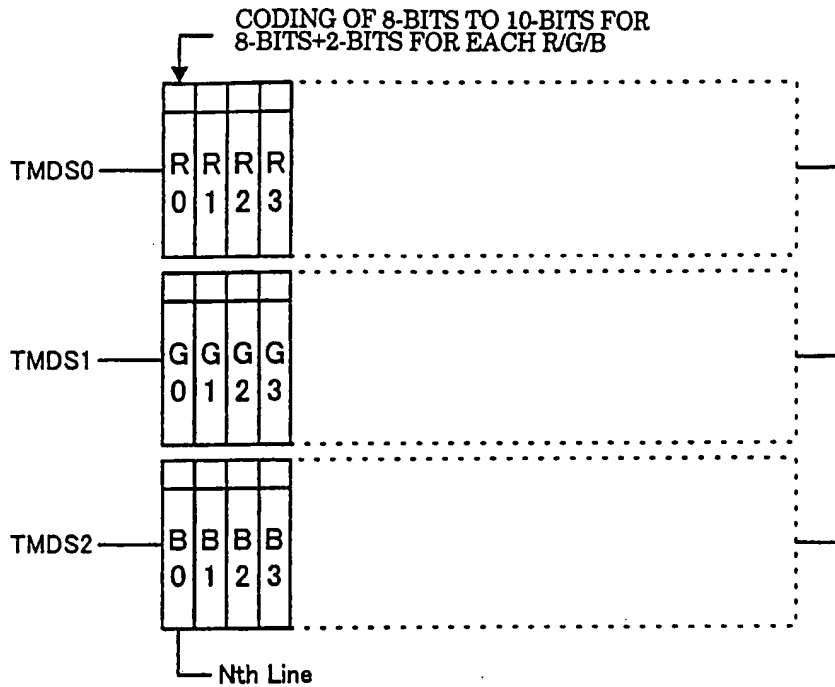
FIG. 16



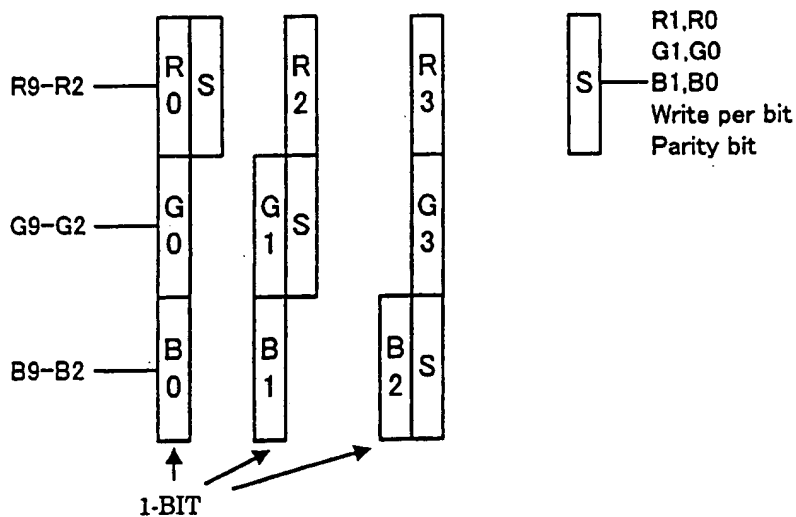
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FIG. 17



(a) TMDS DATA TRANSFER



(b) BIT ASSIGN OF 30-BIT COLOR

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FIG. 18

